Terms used **Resource Description Language** Found **3** of **199,915**

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Relevance scale

1 ABET—a standard for Ada in a test environment
Robert L. McGarvey
December 1990 **Proceedings of the conference on TRI-ADA '90 TRI-Ada '90**
Publisher: ACM Press
Full text available: pdf(838.05 KB) Additional Information: full citation, references

2 An integrated concept for design project planning and design flow control
M. Ryba, U. Baitinger
September 1996 **Proceedings of the conference on European design automation EURO-DAC '96/EURO-VHDL '96**
Publisher: IEEE Computer Society Press
Full text available: pdf(145.83 KB) Additional Information: full citation, references, index terms

3 Automated gathering of Web information: An in-depth examination of agents interacting with search engines
Bernard J. Jansen, Tracy Mullen, Amanda Spink, Jan Pedersen
November 2006 **ACM Transactions on Internet Technology (TOIT)**, Volume 6 Issue 4
Publisher: ACM Press
Full text available: pdf(386.13 KB) Additional Information: full citation, abstract, references, index terms

The Web has become a worldwide repository of information which individuals, companies, and organizations utilize to solve or address various information problems. Many of these Web users utilize automated agents to gather this information for them. Some assume that this approach represents a more sophisticated method of searching. However, there is little research investigating how Web agents search for online information. In this research, we first provide a classification for information agent ...

Keywords: Search engines, Web searching, agent searching

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Terms used **functionality graph** and **resource graph** Found **30** of **199,915**

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Relevance scale

1 Modeling methodology: Resource graphs for modeling large-scale, highly congested systems

Paul Hyden, Lee Schruben, Theresa Roeder
December 2001 **Proceedings of the 33nd conference on Winter simulation WSC '01**
Publisher: IEEE Computer Society
Full text available: pdf(425.35 KB) Additional Information: full citation, abstract, references, citings, index terms

Simulations often execute too slowly to be effective tools for decision-making. In particular, this problem has been found in semiconductor manufacturing where conventional job-driven simulation models explicitly track each lot of wafers as it progresses through the system. While a job-driven simulation model offers some advantages, they inherently execute slowly. This paper explicitly defines resource-driven modeling. Here jobs are implicitly tracked through their resource usage. Resource-drive ...

2 A display and analysis tool for process-resource graphs

M. H. Samadzadeh, B. S. Koshy
January 1996 **ACM SIGOPS Operating Systems Review**, Volume 30 Issue 1
Publisher: ACM Press
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, index terms

This paper describes the design and implementation of a graphical tool called Prograph which enables users to model and analyze operating systems process-resource graphs. The Prograph program enables users to model operating system Process-Resource graphs rapidly, analyze the graphs, and then view the different stages of the deadlock analysis. The deadlock representation and analysis tool Prograph was prototypically evaluated by the students in the graduate level Operating Systems class as well ...

3 Some deadlock properties of computer systems

Richard C. Holt
October 1971 **Proceedings of the third ACM symposium on Operating systems principles SOSP '71**
Publisher: ACM Press
Full text available: pdf(877.77 KB) Additional Information: full citation, abstract, references, citings, index terms

First, a "meta theory" of computer systems is developed so that the terms "process" and

"deadlock" can be defined. Next, "reusable resources" are introduced to model objects which are shared among processes, and "consumable resources" are introduced to model signals or messages passed among processes. Then a simple graph model of computer systems is developed, and its deadlock properties are investigated. This graph model is useful ...

4 Some Deadlock Properties of Computer Systems

Richard C. Holt
September 1972 **ACM Computing Surveys (CSUR)**, Volume 4 Issue 3
Publisher: ACM Press
Full text available: pdf(1.46 MB) Additional Information: full citation, references, citings, index terms

5 Process interactions and system correctness: Some deadlock properties of computer systems

Richard C. Holt
June 1972 **ACM SIGOPS Operating Systems Review**, Volume 6 Issue 1/2
Publisher: ACM Press
Full text available: pdf(1.03 MB) Additional Information: full citation, references

6 Automatic generation of FPGA routing architectures from high-level descriptions

Vaughn Betz, Jonathan Rose
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays FPGA '00**
Publisher: ACM Press
Full text available: pdf(957.37 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a "high-level" FPGA architecture description language which lets FPGA architects succinctly and quickly describe an FPGA routing architecture. We then present an "architecture generator" built into the VPR CAD tool [1, 2] that converts this high-level architecture description into a detailed and completely specified flat FPGA architecture. This flat architecture is the representation with which CAD optimization and visualization modules typic ...

7 CAD for reconfigurable computing: Dynamic FPGA routing for just-in-time FPGA compilation

Roman Lysecky, Frank Vahid, Sheldon X.-D. Tan
June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**
Publisher: ACM Press
Full text available: pdf(73.08 KB) Additional Information: full citation, abstract, references, citings, index terms

Just-in-time (JIT) compilation has previously been used in many applications to enable standard software binaries to execute on different underlying processor architectures. However, embedded systems increasingly incorporate Field Programmable Gate Arrays (FPGAs), for which the concept of a standard hardware binary did not previously exist, requiring designers to implement a hardware circuit for a single specific FPGA. We introduce the concept of a standard hardware binary, using a just-in-time ...

Keywords: FPGA, codesign, configurable logic, dynamic optimization, hardware/software partitioning, just-in-time compilation, place and route, platforms, system-on-a-chip, warp processors

8 Queuing and scheduling: Lexicographic QoS scheduling for parallel I/O

Ajay Gulati, Peter Varman

July 2005 **Proceedings of the seventeenth annual ACM symposium on Parallelism in algorithms and architectures SPAA '05**

Publisher: ACM Press

Full text available: pdf(261.78 KB) Additional Information: full citation, abstract, references, index terms

High-end shared storage systems serving multiple independent workloads must assure that concurrently executing clients will receive a fair or agreed-upon share of system I/O resources. In a parallel I/O system an application makes requests for specific disks at different steps of its computation depending on the data layout and its computational state. Different applications contend for disk access making the problem of maintaining fair allocation challenging.We propose a model for differentiate ...

Keywords: QoS, fair scheduling, lexicographic minimization, parallel I/O, resource allocation, storage virtualization

9 Routing: Solving hard instances of FPGA routing with a congestion-optimal restrained-norm path search space

Keith So

March 2007 **Proceedings of the 2007 international symposium on Physical design ISPD '07**

Publisher: ACM Press

Full text available: pdf(340.91 KB) Additional Information: full citation, abstract, references, index terms

The negotiated congestion mechanism forms the basis of most published FPGA routers today, with many routers projecting congestion and any other requirements onto a scalar search space to evaluate candidate paths. In this paper, we study the numerical stability of these scalar projections as the number of iterations increase. We show that in these scalar search spaces the norm of path costs increase exponentially with the number of iterations, leading to floating-point absorption and represent ...

Keywords: FPGA, negotiated congestion, routability-driven routing

10 Methods for a priori feasible layout generation: Routing architecture exploration for regular fabrics

V. Kheterpal, A. J. Strojwas, L. Pileggi

June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**

Publisher: ACM Press

Full text available: pdf(271.92 KB) Additional Information: full citation, abstract, references, citings, index terms

In an effort to control the parameter variations and systematic yield problems that threaten the affordability of application-specific ICs, new forms of design regularity and structure have been proposed. For example, there has been speculation [6] that regular logic fabrics [1] based on regular geometry patterns [2] can offer tighter control of variations and greater control of systematic manufacturing failures. In this paper we describe a routing framework that accommodates arbitrary descripti ...

Keywords: BEOL, regularity

11 Energy-efficient, utility accrual scheduling under resource constraints for mobile

embedded systems
Haisang Wu, Binoy Ravindran, E. Douglas Jensen, Peng Li
August 2006 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 5 Issue 3
Publisher: ACM Press
Full text available: pdf(408.46 KB) Additional Information: full citation, abstract, references, index terms

We present an energy-efficient, utility accrual, real-time scheduling algorithm called ReUA. ReUA considers an application model where activities are subject to time/utility function time constraints, mutual exclusion constraints on shared non-CPU resources, and statistical performance requirements on individual activity timeliness behavior. The algorithm targets mobile embedded systems where *system-level* energy consumption is also a major concern. For such a model, we consider the schedu ...

Keywords: Real-time systems, energy-efficient scheduling, time/utility functions, utility accrual scheduling

12 Exploiting Loop-Level Parallelism on Coarse-Grained Reconfigurable Architectures Using Modulo Scheduling
Bingfeng Mei, Serge Vernalde, Diederik Verkest, Hugo De Man, Rudy Lauwereins
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society
Full text available: pdf(143.58 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

Coarse-grained reconfigurable architectures have become increasingly important in recent years. Automatic design or compilation tools are essential to their success. In this paper, we present a modulo scheduling algorithm to exploit loop-level parallelism for coarse-grained reconfigurable architectures. This algorithm is a key part of our Dynamically Reconfigurable Embedded Systems Compiler (DRESC). It is capable of solving placement, scheduling and routing of operations simultaneously in a modu ...

13 Energy-aware systems: Energy-efficient, utility accrual scheduling under resource constraints for mobile embedded systems
Haisang Wu, Binoy Ravindran, E. Douglas Jensen, Peng Li
September 2004 **Proceedings of the 4th ACM international conference on Embedded software EMSOFT '04**
Publisher: ACM Press
Full text available: pdf(379.20 KB) Additional Information: full citation, abstract, references, index terms

We present an energy-efficient real-time scheduling algorithm called the *Resource-constrained Energy-Efficient Utility Accrual Algorithm* (or ReUA). ReUA considers an application model where activities are subject to time/utility function-time constraints, resource dependencies including mutual exclusion constraints, and statistical performance requirements including probabilistically satisfied, activity (timeliness) utility bounds. Further, ReUA targets mobile embedded systems where syste ...

Keywords: energy-efficient scheduling, real-time systems, time/utility functions, utility accrual scheduling

14 Real time resource allocation in distributed systems
John Reif, Paul Spirakis
August 1982 **Proceedings of the first ACM SIGACT-SIGOPS symposium on Principles of distributed computing PODC '82**

Publisher: ACM Press

Full text available: pdf(852.77 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we consider a resource allocation problem which is local in the sense that the maximum number of users competing for a particular resource at any time instant is bounded and also at any time instant the maximum number of resources that a user is willing to get is bounded. The problem may be viewed as that of achieving matchings in dynamically changing hypergraphs, via a distributed algorithm. We show that this problem is related to the fundamental problem of < ...

15 An architecture design and assessment system for software/hardware codesign

Connie U. Smith, Geoffrey A. Frank, John L. Cuadrado

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation DAC '85**

Publisher: ACM Press

Full text available: pdf(908.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Codesign of hardware and software for high performance signal processing systems is important if the potential benefits of VLSI are to be realized. This article describes a CAD system developed to support the codesign of hardware and software architectures for high performance digital signal processors which is based on a directed graph methodology. A comprehensive example is developed to demonstrate the use of the system, the fundamentals of the modeling and analysis methodology are discus ...

16 Deadlock prevention, detection, and resolution: an annotated bibliography

Glen Newton

April 1979 **ACM SIGOPS Operating Systems Review**, Volume 13 Issue 2

Publisher: ACM Press

Full text available: pdf(784.98 KB) Additional Information: full citation

17 Synthesis for FPGAs: Three-dimensional place and route for FPGAs

Cristinel Ababei, Hushrav Mogal, Kia Bazargan

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(494.04 KB) Additional Information: full citation, abstract, references, citings

We present timing-driven partitioning and simulated annealing based placement algorithms together with a detailed routing tool for 3D FPGA integration. The circuit is first divided into layers with limited number of inter-layer vias, and then placed on individual layers, while minimizing the delay of critical paths. We use our tool as a platform to explore the potential benefits in terms of delay and wire-length that 3D technologies can offer for FPGA fabrics. Experimental results show on averag ...

18 Floorplanning: Layer assignment for reliable system-on-package

Jacob R. Minz, Sung Kyu Lim

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press

Full text available: pdf(216.18 KB) Publisher Site Additional Information: full citation, abstract, references, citings

The routing environment for the new emerging mixed-signal System-on-Package (SOP) technology is more advanced than that of the conventional PCB or MCM technology -- pins are located at all layers of SOP packaging substrate rather than the top-most layer only. We propose a new interconnect-centric layer assignment algorithm named LA-SOP that handles arbitrary routing topologies and produces near optimal results. The contribution of this work is threefold: (i) modeling of the SOP routing resource, ...

19 Variation and yield: Performance and yield enhancement of FPGAs with within-die variation using multiple configurations

Yohei Matsumoto, Masakazu Hioki, Takashi Kawanami, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa, Hanpei Koike

February 2007 **Proceedings of the 2007 ACM/SIGDA 15th international symposium on Field programmable gate arrays FPGA '07**

Publisher: ACM Press

Full text available: pdf(422.84 KB) Additional Information: full citation, abstract, references, index terms

A new method for improving the timing yield of field-programmable gate array (FPGA) devices affected by random within-die variation is proposed. By selection of an appropriate configuration from a set of functionally equivalent configurations such that the critical paths do not share same circuit resources on the FPGA, both the average critical path delay and its standard deviation are reduced substantially under conditions of large random variation. Large within-die variations of device paramet ...

Keywords: FPGA, configuration, timing yield, within-die variation

20 Net and Pin Distribution for 3D Package Global Routing

Jacob R. Minz, Mohit Pathak, Sung Kyu Lim

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 2 DATE '04**

Publisher: IEEE Computer Society

Full text available: pdf(63.91 KB) Additional Information: full citation, abstract, index terms

In this paper, we study the net and pin distribution problem for global routing targeting three dimensional packaging layout via System-on-Package (SOP). The routing environment for the new emerging mixed-signal SOP technology is more advanced than that of the conventional PCB or MCM technology -- pins are located at all layers of SOP packaging substrate rather than the top-most layer only. This is the first work to formulate and solve the multi-layer net and pin distribution for layer, wireleng ...

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